QRP 2m FM Transceiver Project

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Introduction

The complexity of amateur transceivers reached the point that their construction is generally left to commercial manufacturers. For many radio amateurs the number of components required to build such a project and their assembly often discourage from starting this adventure.

Another question that many amateurs are asking is “why should I build a homebrewed radio when I could buy it paying less and perhaps obtaining more functions ?” and this is for sure a correct question !

Electronic difficulties are accompanied by mechanical problems. Replicating the mechanical aspect of a modern enclosure seems to require a machine shop and the talents of an artist.

There are many difficulties not always easily and economically overcoming but the most important reason which encourages the amateur to start this adventure is the ability to transmit and to receive his voice with an object built with his own hands.

Who builds a homebrewed radio lives on the spirit of Guglielmo Marconi[1], who faced the airwaves with his radio equipments and experiments.

This is my second transceiver, designed with the desire to constantly learn new concepts and experiment with new techniques. I wanted to design a easy to build radio with readily available components. This paper describes the main concepts and the construction of a QRP VHF transceiver on the 2m band (144-148 MHz) designed after many experiments and tests.

I have used all discrete components avoiding the use of SMD components, difficult to solder and replace. This transceiver is based on a microcontroller that governs all the functions. The controller I used is the Parallax Basic Stamp BS2-IC.

The transceiver is based on classic superheterodyne design. It adopts a double conversion narrowband superheterodyne FM receiver with excellent sensitivity achieved by a dual-gate MOSFET. The project of the receiver has been significantly simplified by using a Motorola MC3372 integrated circuit. The frequency stability of the VCO is then achieved using a PLL with reference frequency of 8 MHz, I used a Fujitsu PLL MB1502 working up to 1.1 Ghz.

The transmitter provides about 1.5 W of power into a load of 52 ohms.

I hope you will find this lecture interesting and useful for your next radio creations.

Note: This transceiver may be operated only by radio amateurs as part of their approval.

[1] http://www.nobelprize.org/nobel_prizes/physics/laureates/1909/marconi-bio.html

Technical Data

General

- Frequency range: 144-148 MHz U.S.A. (144-146 Europe)
- Channel spacing: 25kHz
- Power supply: 13.8 V DC ±20% (negative ground)
- Microprocessor PLL controlled

Receiver

- Double-conversion super heterodyne system
- Sensitivity: 0.2vμV typical (at 12dB SINAD)
- Intermediate frequencies: 1st 10.7Mhz, 2nd 455 Khz
- Audio output power
- 1W at 10% distortion at 8Ω

Transmitter

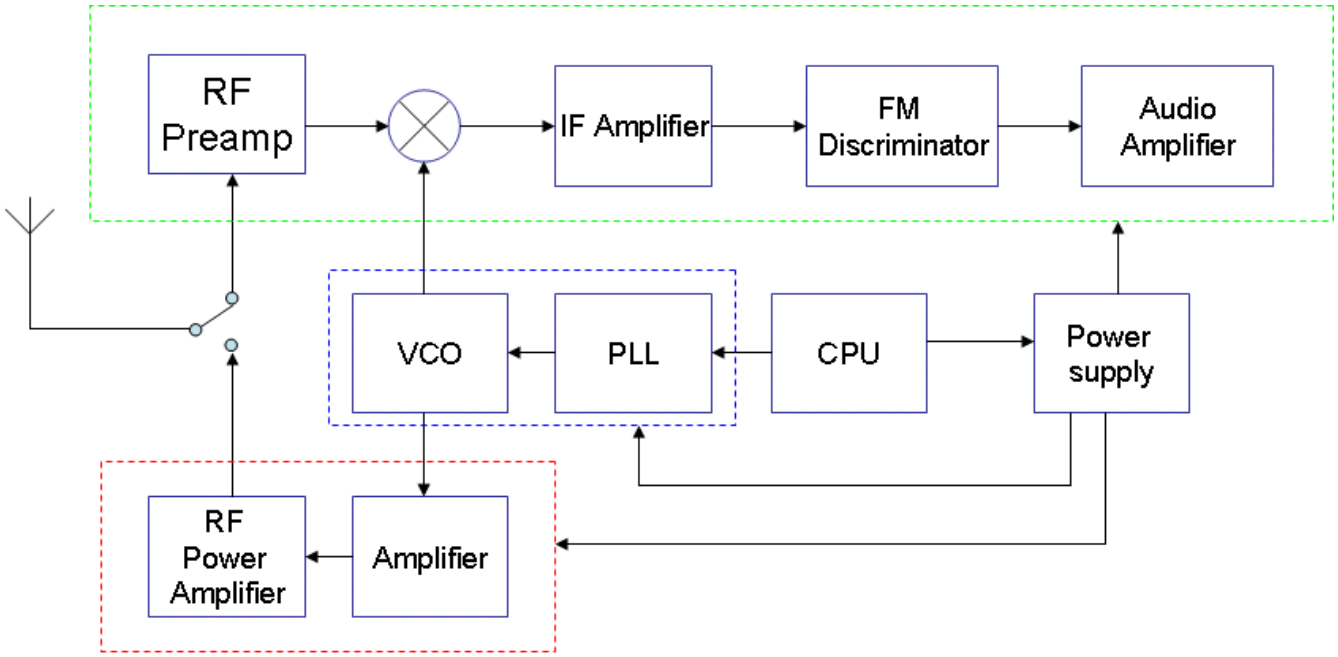
- RF power: 1.5W at 12V

User interface

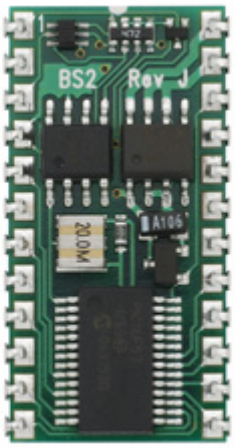
- Button: frequency UP
- Button: frequency DOWN
- Button: MID frequency
- Button: Microphone PTT (push to talk)
- AF gain
- Squelch
- LCD Display
- S-meter for signal reception and power transmission

Circuit description

In this picture you can see the block diagram of the transceiver.



The transceiver is controlled by a Parallax Basic Stamp "BS2-IC" CPU. For any specific and detailed information about this great processor, visit the site: http://www.parallax.com



A BASIC Stamp is a single-board computer that runs the Parallax PBASIC language interpreter. The developer's code is stored in an EEPROM, which can also be used for data storage. The PBASIC language has easy-to-use commands for basic I/O, like turning devices on or off, interfacing with sensors, etc.

More advanced commands let the BASIC Stamp module interface with other integrated circuits, communicate with each other, and operate in networks.

The BASIC Stamp microcontroller has prospered in hobby, lower-volume engineering projects and education due to ease of use and a wide support base of free application resources.

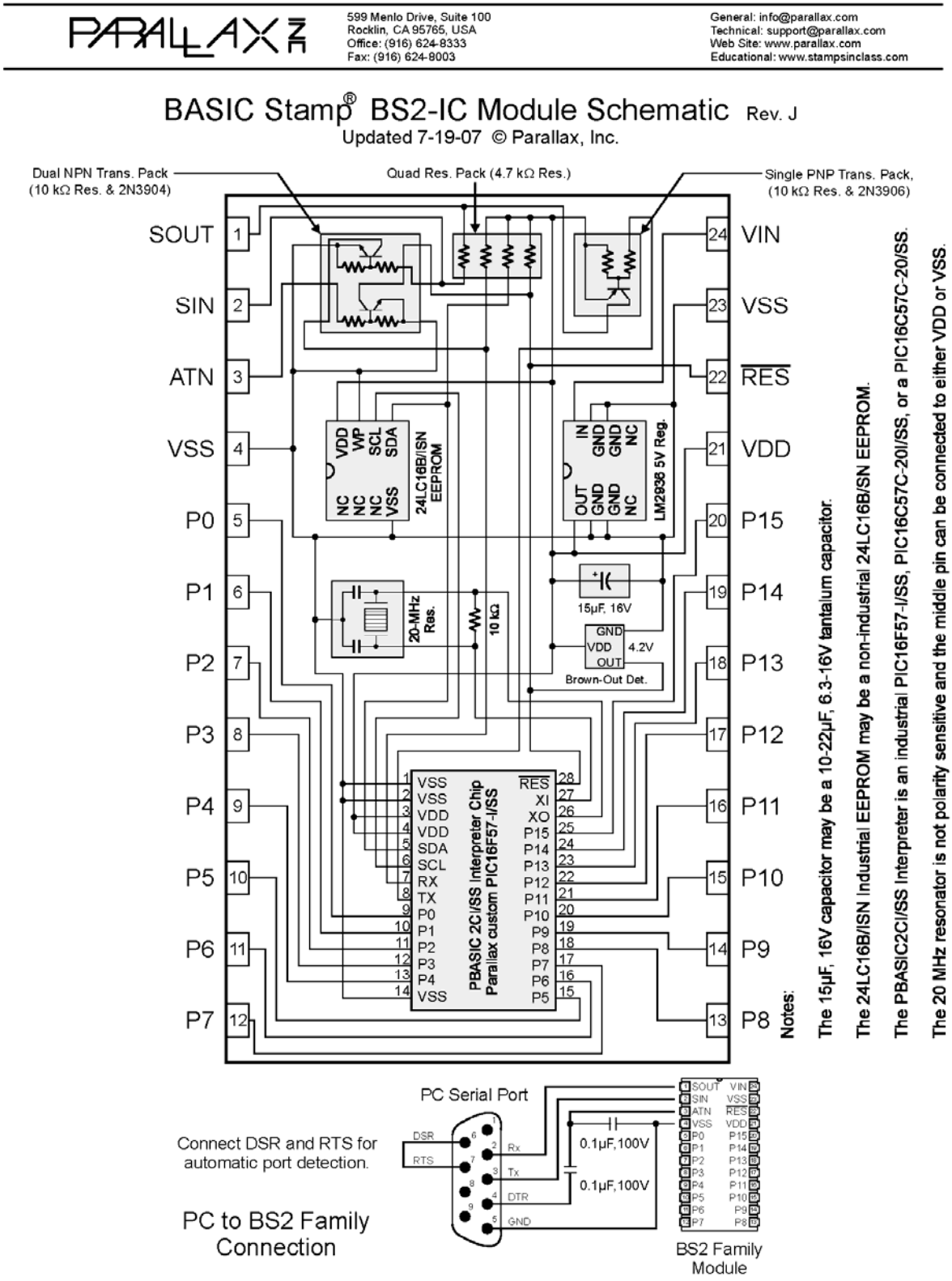


Fig. 2: Basic Stamp schematic diagram

The BS2 controls all functions of the radio: frequency change, muting status, PLL programming, power switching. The firmware is written in PBasic. The user interaction occurs through three input buttons and through a display for displaying messages.

The processor performs these tasks:

- acquires the user's input: frequency change and pressure of the transmissin button (PTT);
- provides power to the various circuits of the radio (transmitter, receiver, PLL-VC);
- programs the registers of the PLL using a synchronous SPI bus (latch Enable, clock, data).

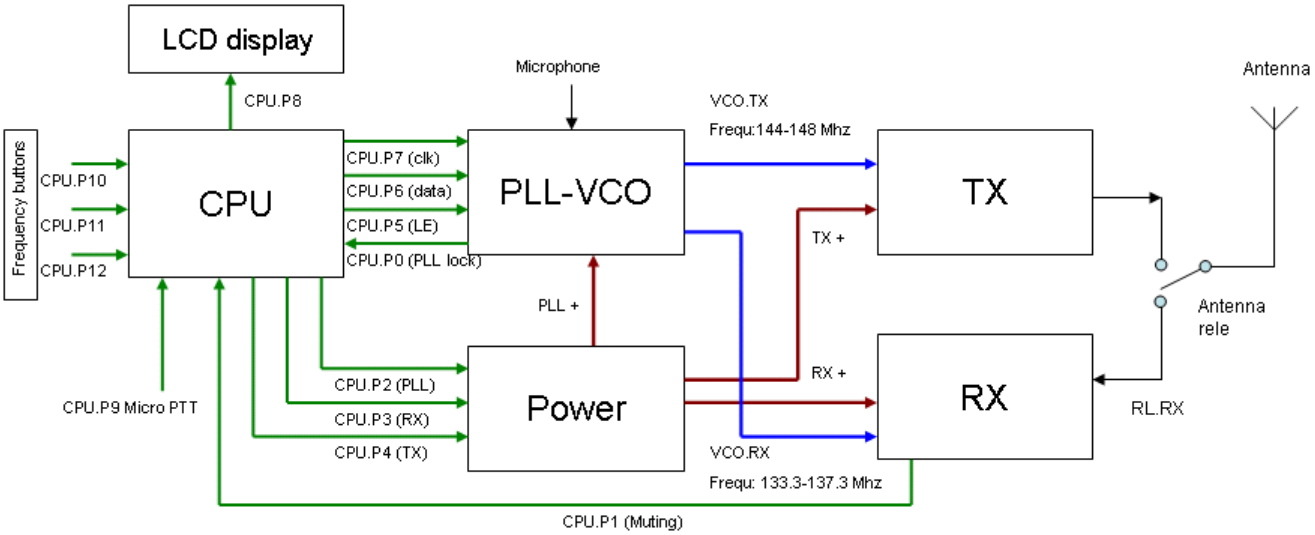


Fig. 3: Main blocks with data / power lines

CPU Pin	Pin name	Signal	Signal direction	0	1
5	P0	PLL lock (from MB1502)	**input**	**Error**	**Lock**
6	P1	Muting status (from MC3772)	**input**	**ON**	**OFF**
7	P2	PLL power	**output**	**OFF**	**ON**
8	P3	RECEIVER power	**output**	**OFF**	**ON**
9	P4	TRANSMITTER power	**output**	**OFF**	**ON**
10	P5	PLL LE	**output**	**NA**	**NA**
11	P6	PLL data	**output**	**NA**	**NA**
12	P7	PLL clock	**output**	**NA**	**NA**
13	P8	Serial display	**output**	**NA**	**NA**
14	P9	Button frequency DOWN	**input**	**PRESSED**	
15	P10	Button MID frequency	**input**	**PRESSED**	
16	**P11**	**Button frequency UP**	**input**	**PRESSED**	

Fig. 4: CPU lines description

Operations

When you power the radio on this goes in receive mode and tunes itself to the low band limit frequency (144 MHz), then It enters in a loop that controls the PTT button and the buttons that change frequency.

Reception (RX):
1) the CPU turns **on** the PLL circuit: P2 =1;
2) the CPU communicates to the PLL parameters N and A through P5, P6, P7 lines;
3) the CPU turns **on** the receiving circuit: P3=1.

Frequency change UP (the radio is in reception mode):
1) communicates to the PLL the parameters N and A through P5, P6, P7 lines;
2) updates the frequency on LCD Display (P8 line).

Frequency change DOWN (the radio is in reception mode):
1) communicates to the PLL the parameters N and A through P5, P6, P7 lines;
2) updates the frequency on LCD Display (P8 line).

Transmission (TX):
1) The CPU detects PTT button activation P9=0;
2) turns **off** the RX circuit: P3=0;
3) communicates to the PLL the parameters N and A through P5, P6, P7 lines;
4) turns **on** the TX circuit: P4=1.

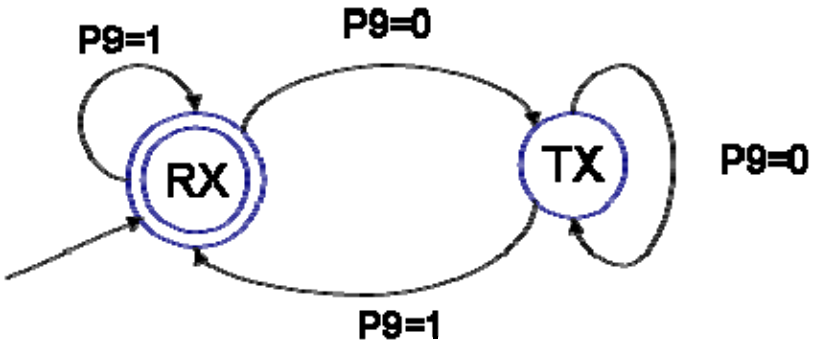


Fig. 5: finite automata representing the states: RX and TX

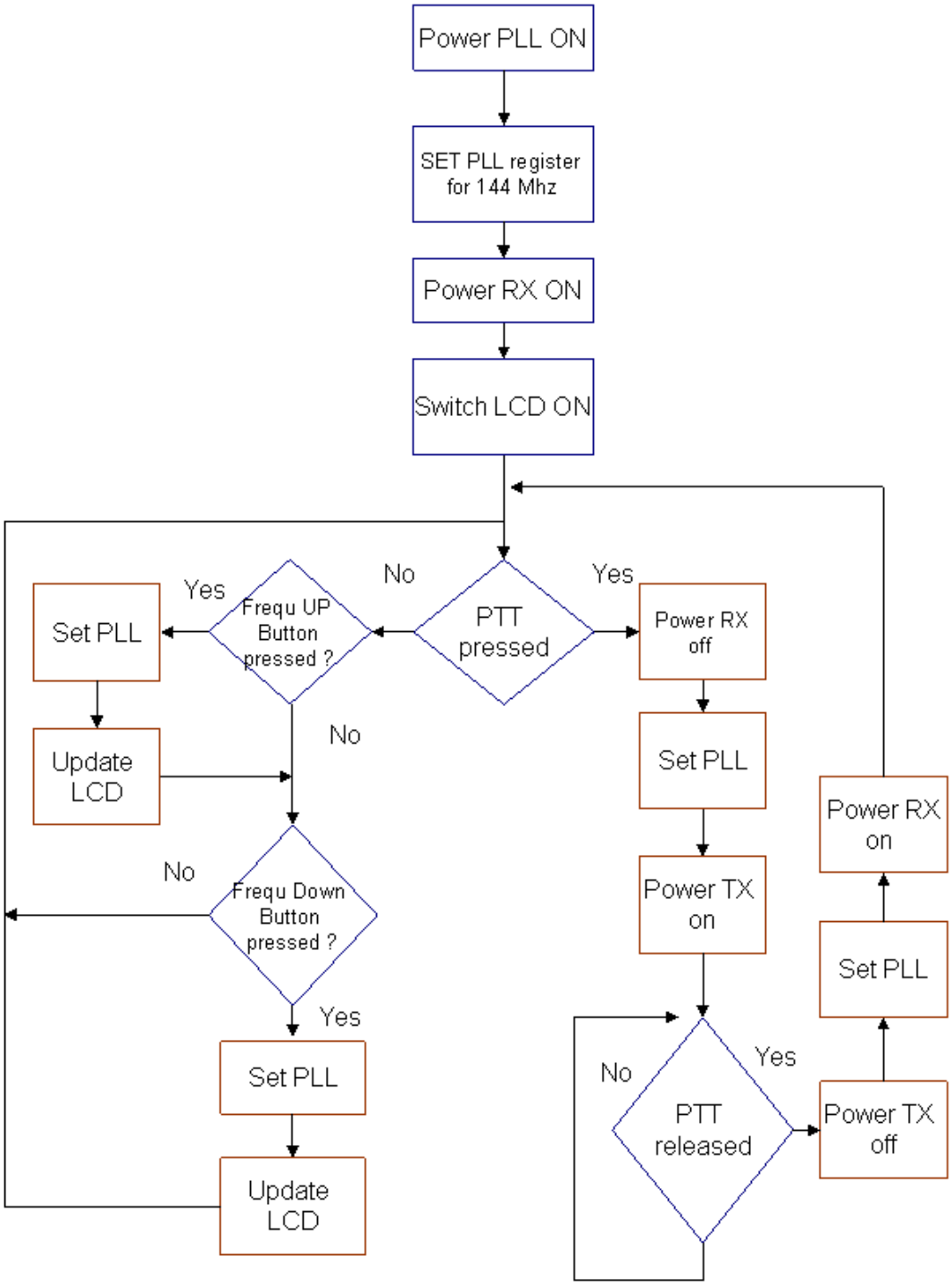


Fig. 6: software flowchart

Receiver

The principle of operation of the superheterodyne receiver depends on the use of frequency mixing. The signal from the antenna is filtered to reject the image frequency and then is amplified. A local oscillator (VCO) produces a sine wave which mixes with signal from antenna, shifting it to a specific intermediate frequency (IF), usually a lower frequency. The IF signal is itself filtered and amplified and possibly processed in additional ways. The demodulator uses the IF signal rather than the original radio frequency to recreate a copy of the original modulation (audio).

The radio signal coming from the antenna is very small, often only a few microvolts, this will be tuned with **L1, C3** and amplified with a Mosfet **MSFT1**. One more tuned circuit **L2, C4** at this stage blocks frequencies which are far from the intended reception frequency. The signal is then fed into a circuit build around the Mosfet **MSFT2** where it is mixed with a sine wave from a variable controlled oscillator known as VCO (POS-200). The mixer produces both sum and difference beat frequencies signals, each one containing the modulation contained in the desired signal. The output of the mixer includes the original RF signal at f_d, the local oscillator signal at f_{LO}, and the two new frequencies f_d+f_{LO} and f_d-f_{LO}.

The mixer may inadvertently produce additional frequencies such as 3rd and higher-order intermodulation products. The undesired signals are removed by the IF bandpass filter **XF1**, leaving only the desired offset IF signal at f_{IF} (10.7 Mhz) which contains the original modulation (transmitted information) as the received radio signal had at f_d.

The next stage is the intermediate frequency amplifier **TR1** that is tuned to the specific frequency of 10.7 Mhz not dependent on the receiving frequency. The 10.7 Mhz signal is entered in the discriminator stage **IC2** (MC3372).

The MC3372 performs single conversion FM reception and consists of an oscillator, mixer, limiting IF amplifier, quadrature discriminator, active filter, squelch switch, and meter drive circuitry. This device is designed for use in FM dual conversion communication equipment.

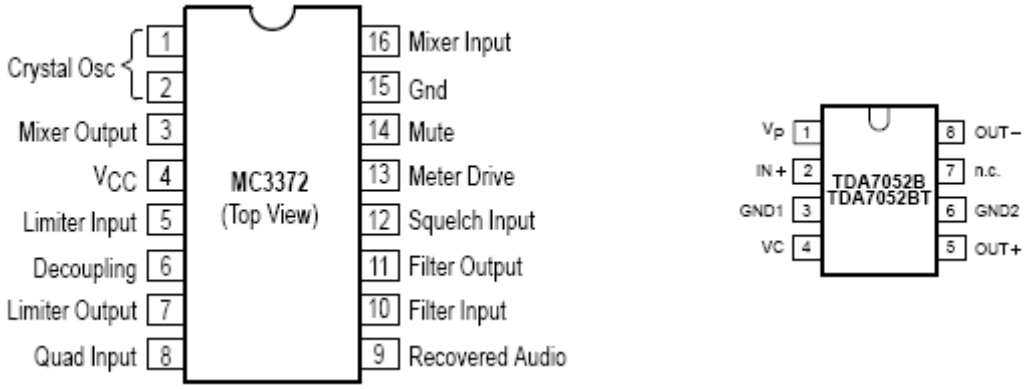


Fig. 7: MC3372 and TDA7052 pinout

The MC3372 is similar to the MC3361/MC3357 FM IFs, except that a signal strength indicator replaces the scan function controlling driver which is in the MC3361/MC3357.

The muting function is implemented connecting the pin 14 (Mute) to the pin 4 of the TDA7052. A transistor **TR3** communicates to the CPU the status of this line.

Transmitter

The signal from the VCO is amplified by the MAV-11 before being sent to the final stage **TR11**. The audio modulation it performed using a transistor **TR4** that amplifies the signal coming from the microphone.

PLL– VCO

A voltage-controlled oscillator or VCO is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. The frequency of oscillation is varied by the applied DC voltage, while modulating signals may also be fed into the VCO to cause frequency modulation (FM).

The VCO used in this RTX is the **POS-200** from Mini-Circuits.

Electrical Specifications

MODEL NO.	FREQ. (MHz)		POWER OUTPUT (dBm)	TUNING VOLTAGE (V)		PHASE NOISE dBc/Hz SSB at offset frequencies: Typ.				PULLING pk-pk @ 12 dBr (MHz)	PUSHING (MHz/V)	TUNING SENSI-TIVITY (MHz/V)	HARMONICS (dBc)		3 dB MODULATION BANDWIDTH (MHz)	DC OPERATING POWER	
	Min.	Max.	Typ.	Min.	Max.	1 kHz	10 kHz	100 kHz	1 MHz	Typ.	Typ.	Typ.	Typ.	Max.	Typ.	Vcc (volts)	Current (mA) Max.
POS-200(+)	100	200	+10	1	16	-80	-102	-122	-142	1.0	0.2	7.1-8.6	-24	-20	0.1	12	20

Fig. 8: POS-200 functional data

The VCO generates a signal within the 144-148 Mhz (144-146 Mhz in Europe) frequency range for the transmission and within the 133.3-137.3 Mhz frequency range for the reception. The VCO output is connected to the receiver mixer and to the MAV-11 amplifier for the transmitter. The VCO circuit is always active. In reception mode the receiver part is powered by the microprocessor and the VCO injects its signal in the mixer. In transmission mode the receiving part is switched off, the PLL is updated with the parameters required to produce frequencies from 144 to 148 MHz and the transmitter is switched on.

The VCO is controlled by the PLL (Phase Locked Loop). The main blocks inside a PLL are: the comparator phase (Phase Detector), the low pass filter PB (loop filter), the VCO (Voltage Controlled Oscillator) and the reference oscillator.

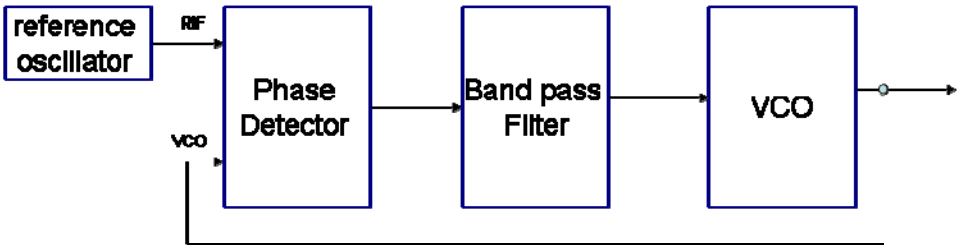


Fig. 9: PLL description

In principle, a PLL is a device that locks the phase or the frequency of an output signal to a reference. At the operational level, therefore, the phase comparator makes a comparison between

the phase reference signal and the signal output from the VCO and generates a voltage whose average value is proportional to the phase shift of the two signals.

The output signal from the phase comparator is then a square wave with a variable duty-cycle and is up to the low pass filter to extract only the component continues to be applied to the oscillator voltage-controlled VCO. As can be seen on the diagram the entire system is negative feedback that tends to stabilize the VCO frequency equal to the input of reference but, as a result of hardware used in the phase comparators, the two signals, there will usually be a fixed phase difference, the previous situation goes under the name of "signal lock".

The Fujitsu MB1502 PLL, utilizing BI-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function. The MB1502 contains a 1.1GHz two modulus prescaler that can select of either 64/65 or 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter) and analogue switch to speed up lock up time.

PLL parameters

The microcontroller BS2-IC communicates with the PLL using three data lines (Latch enable, Data, Clock). The synchronous serial protocol (SPI) is used to load data into the latch R, N, A and SW registers. The data must be transferred in this order:

1) registers SW, R;
2) control bit C=1;
3) clock pulse (PULSOUT);
4) registers N, A;
5) control bit C=0;
6) clock pulse (PULSOUT).

With this procedure each value is loaded in the respective latch that stores and provides the corresponding divisor.

```
SHIFTOUT DataPin, ClockPin, MSBFIRST, [1\1]      ' BIT SW
SHIFTOUT DataPin, ClockPin, MSBFIRST, [640\14]   ' register R
SHIFTOUT DataPin, ClockPin, MSBFIRST, [1\1]      ' bit C=1
PULSOUT LatchEnablePin, 15

SHIFTOUT DataPin, ClockPin, MSBFIRST, [N\11]     ' LOAD N
SHIFTOUT DataPin, ClockPin, MSBFIRST, [A\7]      ' LOAD A
SHIFTOUT DataPin, ClockPin, MSBFIRST, [0\1]      ' bit C=0
PULSOUT LatchEnablePin, 15
```

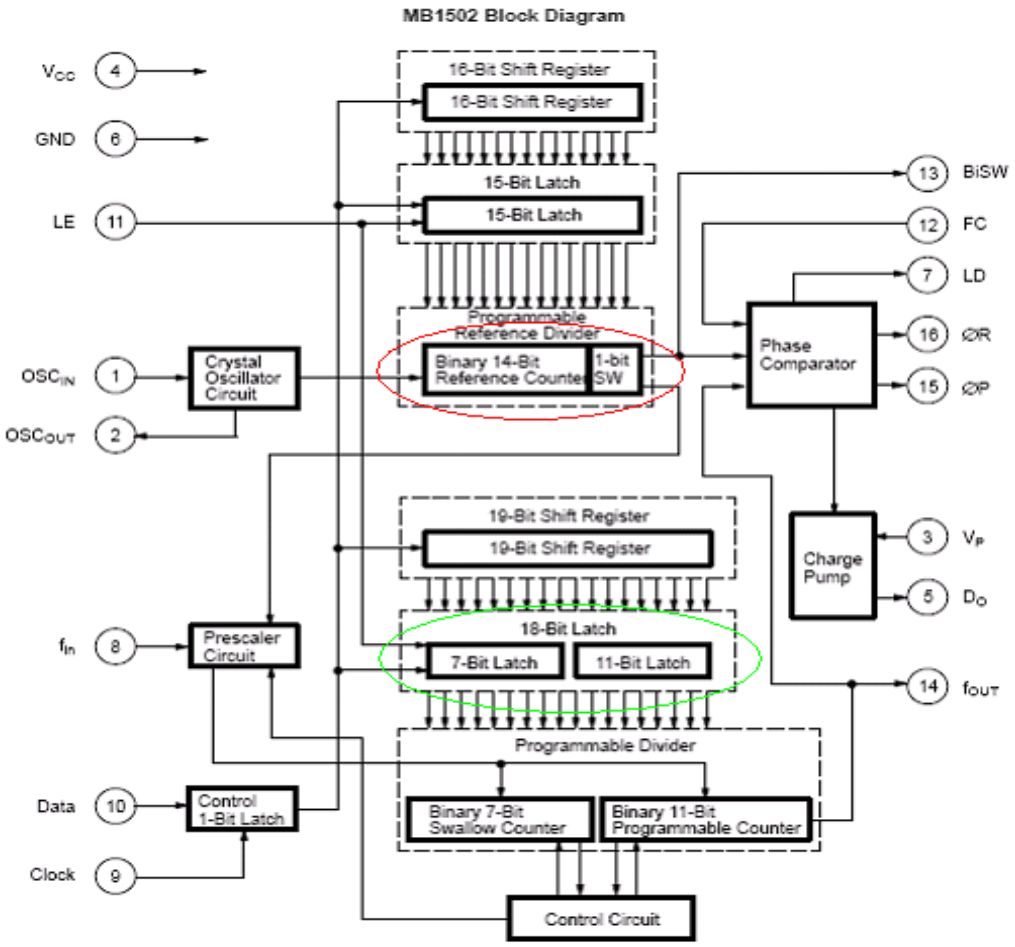


Fig. 10: MB1502 internal registers

How to calculate the N and A values ?

Let's do an example. Supposing we want to know the N and A paramenters for a 145 Mhz frequency:

RIF = 12.5 Khz = 12500 Hz
P = 64
F = 145 Mhz = 145000000Hz

$$F_{VCO} = RIF \cdot [(P \cdot N) + A]$$

To compute N and A:

Division factor: $F_{DC} = \frac{F_{VCO}}{P \cdot RIF} = \frac{145000000}{64 \cdot 12.5} = 181.25$

N = integer part(F_{DC}) = integer part(181.25) = **181**
A =P * decimal(F_{DC}) = 64*0.25 = **16**

Registers N and A for each frequency

Transmission			Reception		
Frequency	**N**	**A**	**Frequency**	**N**	**A**
144,000	180	0	133,300	166	40
144,025	180	2	133,325	166	42
144,050	180	4	133,350	166	44
144,075	180	6	133,375	166	46
144,100	180	8	133,400	166	48
144,125	180	10	133,425	166	50
144,150	180	12	133,450	166	52
144,175	180	14	133,475	166	54
144,200	180	16	133,500	166	56
144,225	180	18	133,525	166	58
144,250	180	20	133,550	166	60
144,275	180	22	133,575	166	62
144,300	180	24	133,600	167	0
144,325	180	26	133,625	167	2
144,350	180	28	133,650	167	4
144,375	180	30	133,675	167	6
144,400	180	32	133,700	167	8
144,425	180	34	133,725	167	10
144,450	180	36	133,750	167	12
144,475	180	38	133,775	167	14
144,500	180	40	133,800	167	16
144,525	180	42	133,825	167	18
144,550	180	44	133,850	167	20
144,575	180	46	133,875	167	22
144,600	180	48	133,900	167	24
144,625	180	50	133,925	167	26
144,650	180	52	133,950	167	28
144,675	180	54	133,975	167	30
144,700	180	56	134,000	167	32
144,725	180	58	134,025	167	34
144,750	180	60	134,050	167	36
144,775	180	62	134,075	167	38
144,800	181	0	134,100	167	40
…	**…**	**…**	**…**	**…**	**…**
…	**…**	**…**	**…**	**…**	**…**
147,825	184	50	137,125	171	26
147,850	184	52	137,150	171	28
147,875	184	54	137,175	171	30
147,900	184	56	137,200	171	32
147,925	184	58	137,225	171	34
147,950	184	60	137,250	171	36
147,975	184	62	137,275	171	38
148,000	**185**	**0**	**137,300**	**171**	40

Fig. 11: PLL parameters datasheet

Schematics

The circuit diagram is spread over five figures. Figure 1 shows the CPU circuit, Figure 2 the PLL schematic, Figure 3 the receiver schematic, Figure 4 the transmitter circuit and Figure 5 the power commutation circuit.

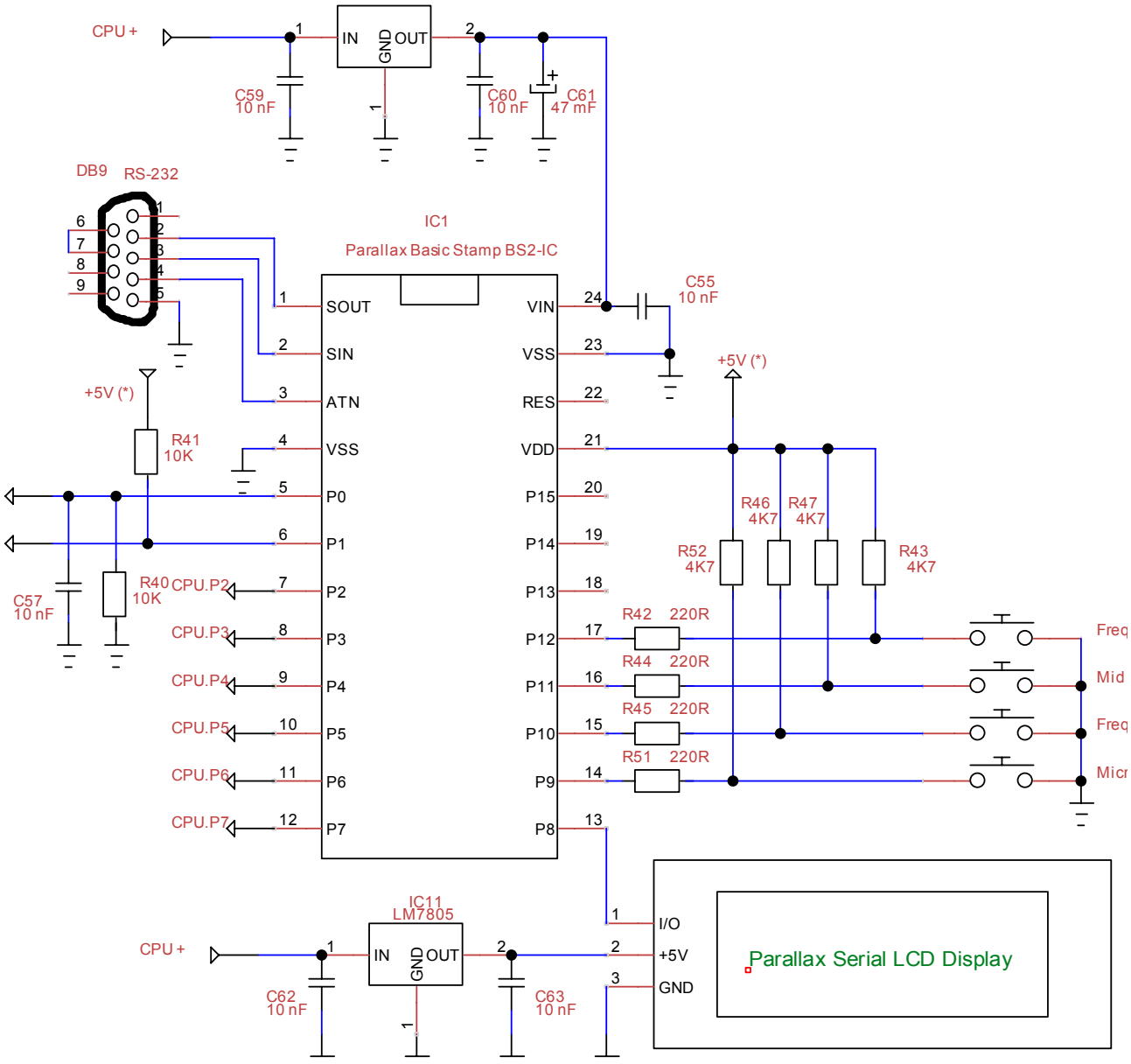


Figure 13: CPU

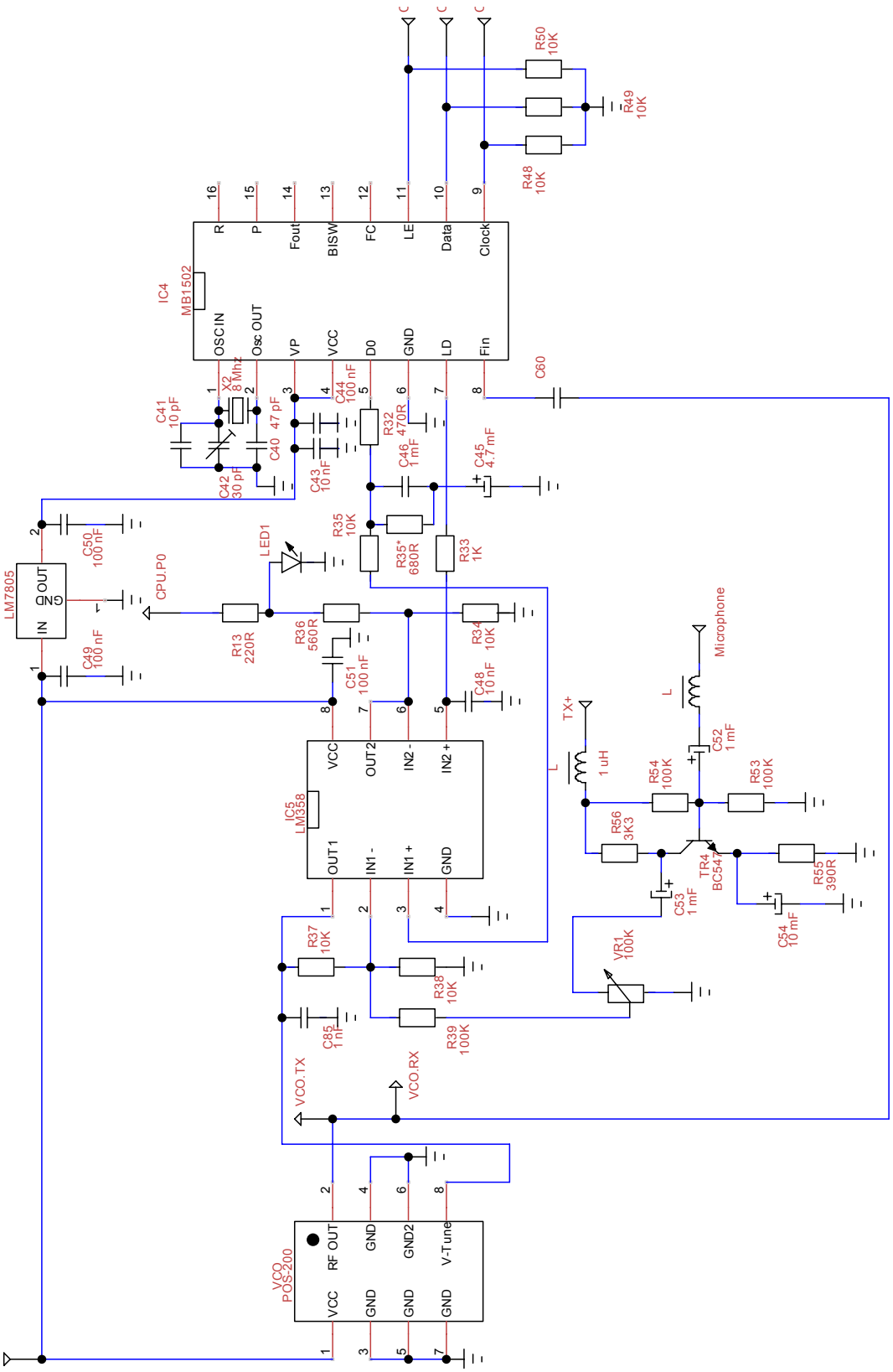


Figure 14: PLL

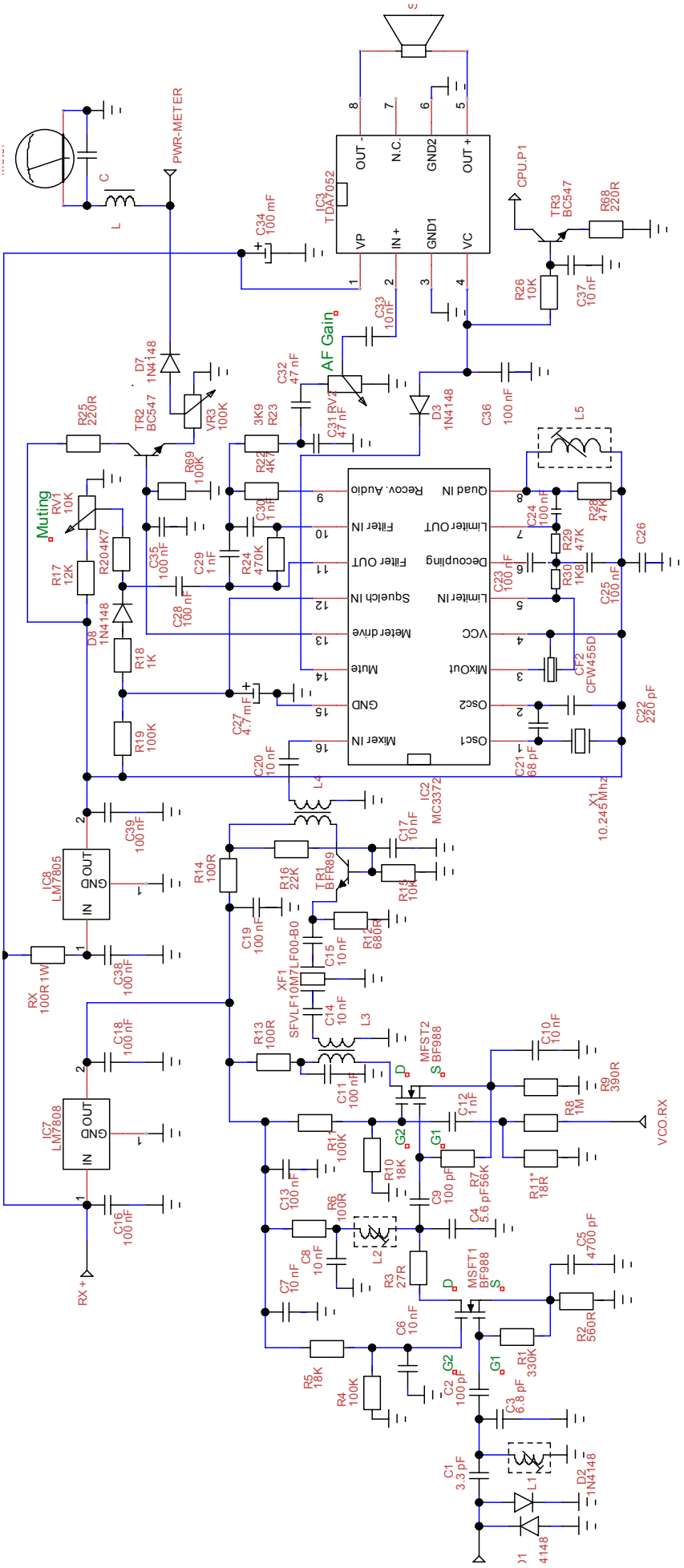


Figure 15: receiver

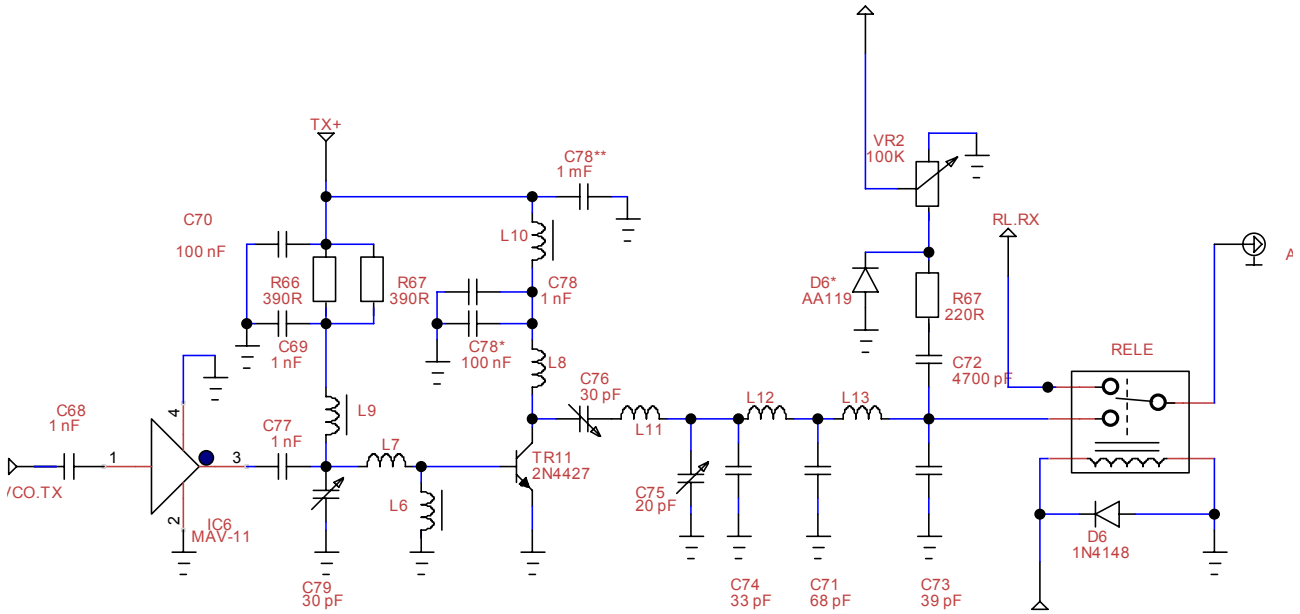


Figure 16: transmitter

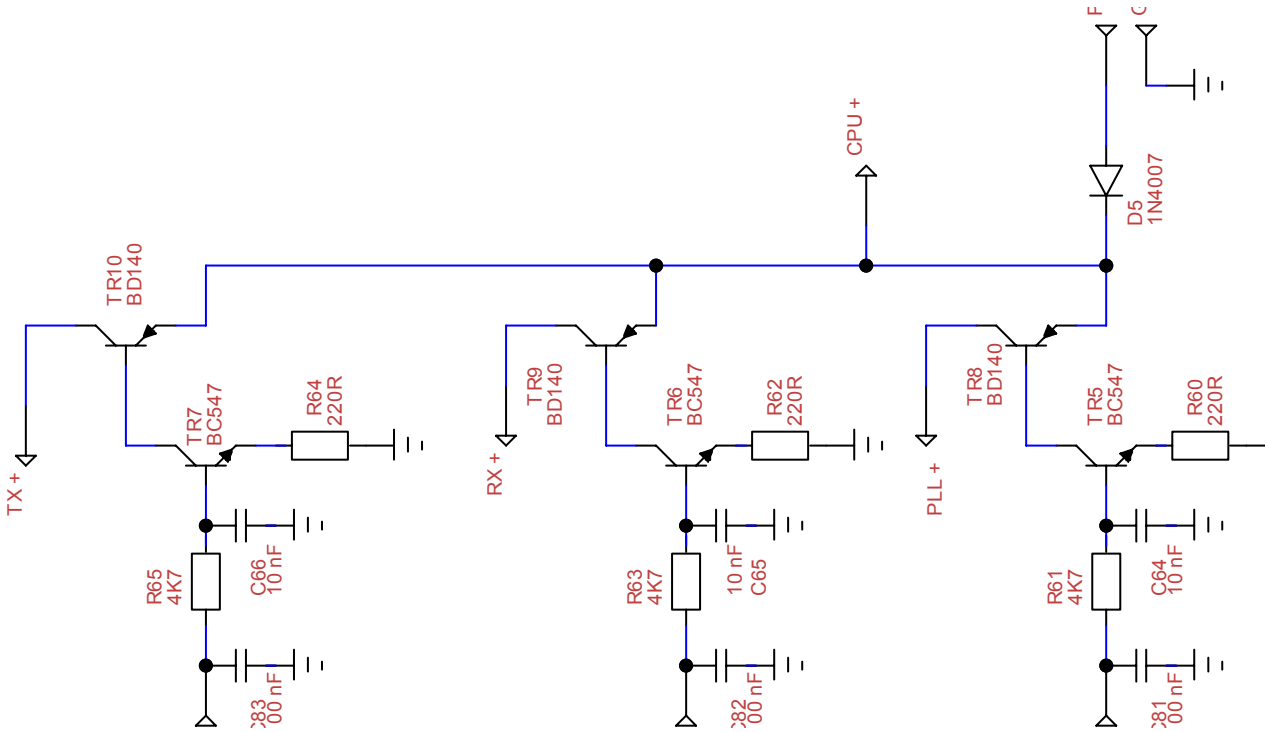


Figure 17: Power commutation

Parts List

Capacitors

C46,C52,C53,C78**	4	1 mF
C12,C29,C30,C68,C69,C77, C78,C85	8	1 nF
C54	1	10 mF
C10,C14,C15,C17,C20,C33, C37,C43,C48,C55,C57,C59, C6,C60,C62,C63,C64,C65, C66,C7,C8	21	10 nF
C41,C60	2	10 pF
C34	1	100 mF electrolytic
C,C11,C13,C16,C18,C19, C23,C24,C25,C26,C28,C35, C36,C38,C39,C44,C49,C50, C70,C78*,C81,C82,C83	23	100 nF
C51	1	220 mF
C2,C9	2	100 pF
C75	1	20 pF
C22	1	220 pF
C1	1	3.3 pF
C42,C76,C79	3	30 pF variable capacitor
C74	1	33 pF
C73	1	39 pF
C27,C45	2	4.7 mF electrolytic
C61	1	47 mF electrolytic
C31,C32	2	47 nF
C40	1	47 pF
C5,C72	2	4700 pF
C4	1	5.6 pF
C3	1	6.8 pF
C21,C71	2	68 pF

Resistors

R11,R19,R39,R4,R53, R54,R69,RV2,VR1,VR2,VR3	11	100K 1/6 W
R13,R14,R6	3	100R 1/6 W
RX	1	100R 1 W
R15,R26,R34,R35,R37,R38, R40,R41,R48,R49,R50,RV1	12	10K 1/6 W
R17	1	12K 1/6 W
R5, R10	2	18K 1/6 W
R11*	1	18R 1/6 W
R18,R33	2	1K 1/6 W
R30	1	1K8 1/6 W
R8	1	1M 1/6 W
R13,R25,R42,R44,R45,R51, R60,R62,R64,R67,R68	11	220R 1/6 W
R16	1	22K 1/6 W
R3	1	27R 1/6 W
R1	1	330K 1/6 W
R55,R66,R67,R9	4	390R 1/6 W
R56	1	3K3 1/6 W
R23	1	3K9 1/6 W
R24	1	470K 1/6 W

R32	1	470R 1/6 W
R28,R29	2	47K 1/6 W
R20,R22,R43,R46,R47,R52, R61,R63,R65	9	4K7 1/6 W
R2,R36	2	560R 1/6 W
R7	1	56K 1/6 W
R12,R35*	2	680R 1/6 W

Transistors

TR1	1	BFR89
TR2,TR3,TR4,TR5,TR6,TR7	6	BC547
TR8,TR9, TR10	3	BD140
TR11	1	2N4427

Crystals

X1	1	10.245 Mhz
X2	1	8 Mhz

Mosfet

MFST2,MSFT1	2	BF988

Integrated Circuits

IC5	1	LM358
IC11,IC8,IC9	3	LM7805
IC7	1	LM7808
IC10	1	LM7809
IC6	1	Mini-Circuits MAV-11
IC4	1	Fujitsu MB1502
IC2	1	Motorola MC3372
IC1	1	Basic Stamp BS2-IC, Parallax item code **BS2-IC**
IC3	1	Philips TDA7052

Diodes

D5	1	1N4007
D6*	1	AA119
D1,D2,D3,D6,D7,D8	6	1N4148

Coils

L1,L2	2	Coilcraft 146-04J08SL
L3,L4	2	10.7 Mhz green IF
L5	1	455 Khz black IF
L6,L9	2	0.33 uH
L7,L8	2	3 turns on air (diameter 4 mm) wire 0.8 mm
L11,L12,L13,L7	3	4 turns on air (diameter 4 mm) wire 0.8 mm
L,L10	2	1 uH

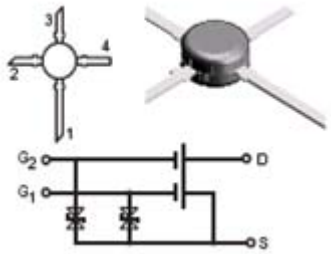
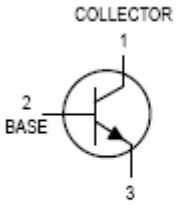
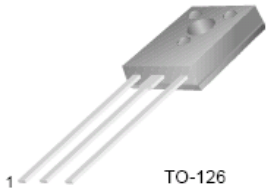
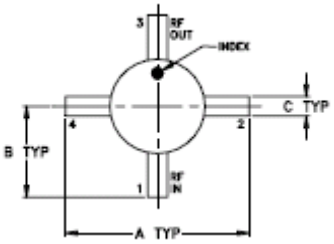
Ceramic filters

CF1	1	Murata SFVLF10M7LF00-B0
CF2	1	Murata CFW455D

Miscellaneus

VCO	1	Mini-Circuits POS-200
SP	1	8 ohm SPEAKER
Meter	1	Meter
LCD	1	4x20 Serial LCD (Backlit), Parallax item code **27979**
RELE	1	12V two ways rele
LED1	1	LED

Semiconductors outline drawings

Component	Outline drawing
BF988	 1 = Drain, 2 = Source, 3 = Gate 1, 4 = Gate 2
BFR99	  Bottom view
BC547	 CASE 29–04, STYLE 17 TO–92 (TO–226AA)
BD140	 TO-126 1. Emitter 2.Collector 3.Base
MAV-11	

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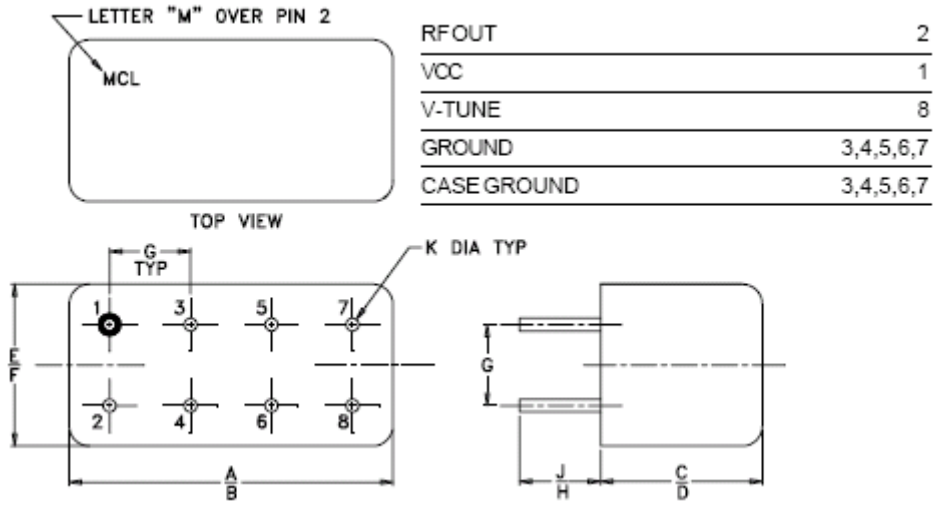
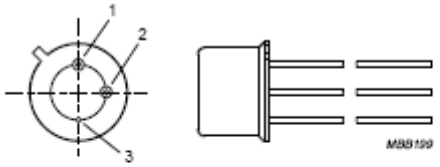
POS-200



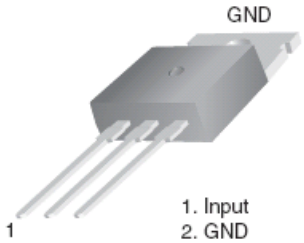
RF OUT	2
VCC	1
V-TUNE	8
GROUND	3,4,5,6,7
CASE GROUND	3,4,5,6,7

2N4427



PIN	DESCRIPTION
1	emitter
2	base
3	collector

LM780XX



1. Input
2. GND
3. Output

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PCB layout

The PCB was designed using Sprint Layout Software, it is a double face circuit.

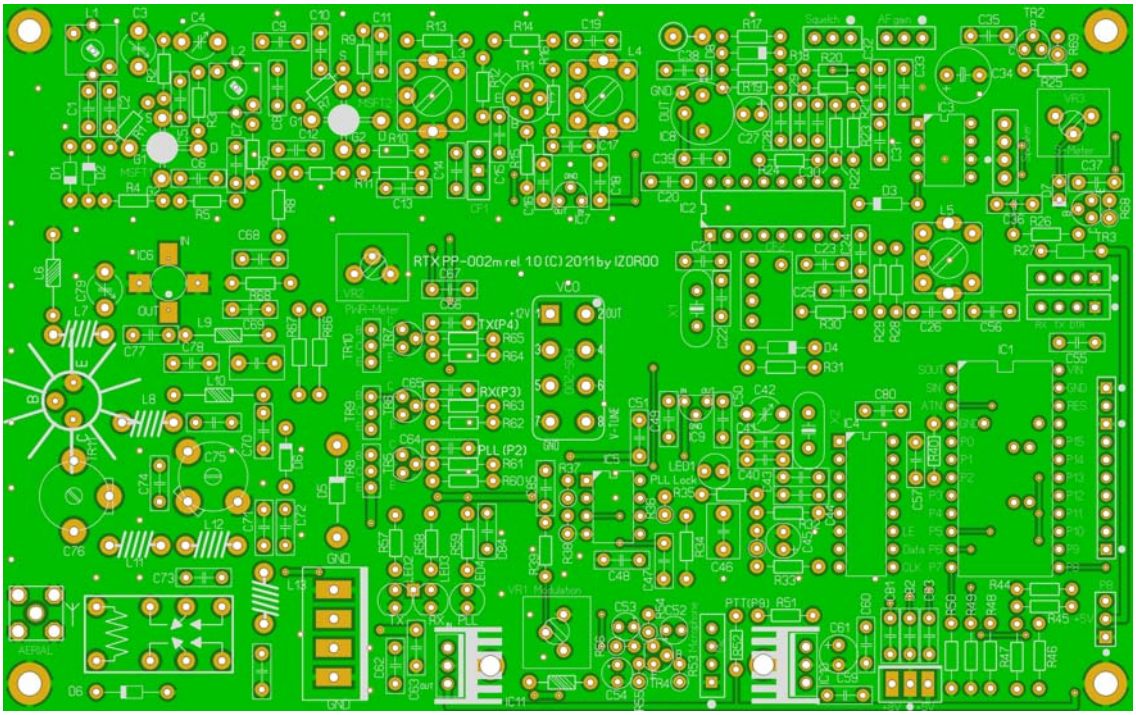


Fig. 18: PCB Front view

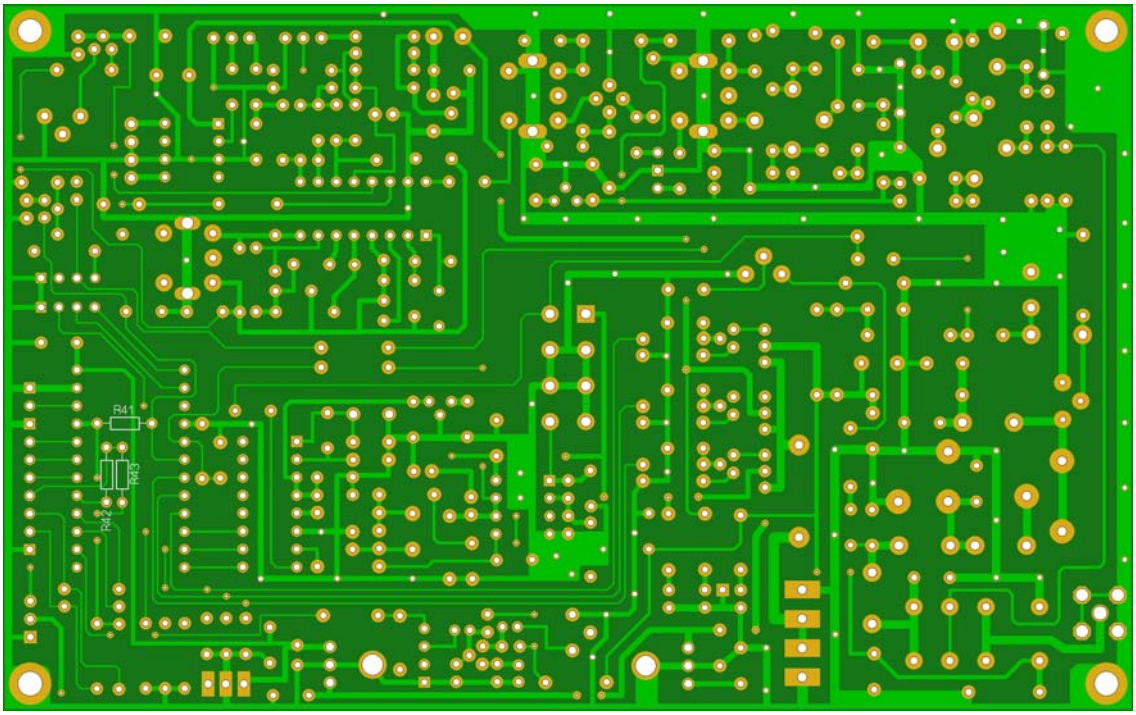


Fig. 19: PCB back view

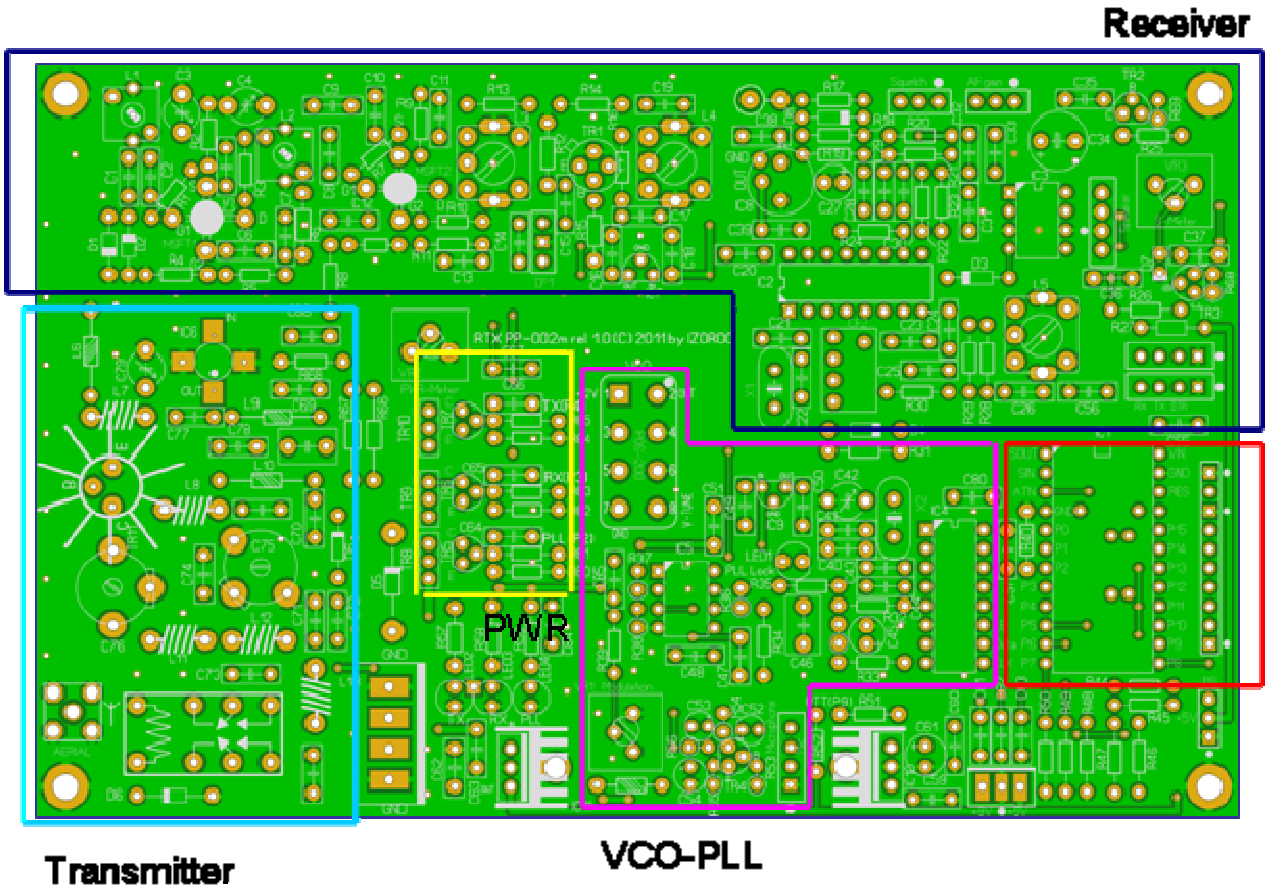


Fig. 20: functional blocks on PCB

Firmware

```
' =============================================================================
'
'   File..... PP-002m  PP-002m.bs2
'   Purpose... (144-148 Mhz) 2m RTX Firmware
'   Author.... IZ0ROO, Paolo Pinto
'   E-mail.... iz0roo@fastwebnet.it
'   Started... 09-01-2011
'   Updated... 09-20-2011
'
'   {$STAMP BS2}
'   {$PBASIC 2.5}
'
' =============================================================================


' Serial baud rates
#SELECT $STAMP
  #CASE BS2, BS2E, BS2PE
    T2400       CON     396
    T9600       CON     84
    T19K2       CON     32
  #CASE BS2SX, BS2P
    T2400       CON     1021
    T9600       CON     240
    T19K2       CON     110
#ENDSELECT
LcdBaud         CON     T19K2

' Parallax Serial LCD pin
LCD PIN 8

LcdBkSpc        CON     $08             ' move cursor left
LcdRt           CON     $09             ' move cursor right
LcdLF           CON     $0A             ' move cursor down 1 line
LcdCls          CON     $0C             ' clear LCD (use PAUSE 5 after)
LcdCR           CON     $0D             ' move pos 0 of next line
LcdBLon         CON     $11             ' backlight on
LcdBLoff        CON     $12             ' backlight off
LcdOff          CON     $15             ' LCD off
LcdOn1          CON     $16             ' LCD on; cursor off, blink off
LcdOn2          CON     $17             ' LCD on; cursor off, blink on
LcdOn3          CON     $18             ' LCD on; cursor on, blink off
LcdOn4          CON     $19             ' LCD on; cursor on, blink on
LcdLine1        CON     $80             ' move to line 1, column 0
LcdLine2        CON     $94             ' move to line 2, column 0
LcdLine3        CON     $A8             ' move to line 2, column 0
LcdLine4        CON     $BC             ' move to line 2, column 0
LcdCC0          CON     $F8             ' define custom char 0
LcdCC1          CON     $F9             ' define custom char 1
LcdCC2          CON     $FA             ' define custom char 2
LcdCC3          CON     $FB             ' define custom char 3
LcdCC4          CON     $FC             ' define custom char 4
LcdCC5          CON     $FD             ' define custom char 5
LcdCC6          CON     $FE             ' define custom char 6
LcdCC7          CON     $FF             ' define custom char 7


muting PIN 1
INPUT muting


' assigns PLL spi bus lines
ClockPin            PIN     7   ' MB1504 clock pin
DataPin             PIN     6   ' MB1504 data  pin
LatchEnablePin      PIN     5   ' MB1504 latch pin

' PLL registers and parameters
N1        VAR   Byte
N2        VAR   Byte
N         VAR   Byte
A         VAR   Word
A1        VAR   Word
A2        VAR   Word
TMP       VAR   Byte
TMP2       VAR   Byte

LOW LatchEnablePin    ' initialize latch output


' Frequency range
LFrequ    VAR   Word
HFrequ    VAR   Word
FStep   VAR   Word
Frequ     VAR   Word
```

```
Frequ2    VAR   Word

LFrequ=44000-10700
HFrequ=48000-10700
Frequ=LFrequ

' Assigns buttons to BS2 pins
pttBtn PIN 9
pttBtnWrk VAR Byte

upBtn PIN 11
upBtnWrk VAR Byte

midBtn PIN 12
midBtnWrk VAR Byte

downBtn PIN 10
downBtnWrk VAR Byte


TXState VAR Byte


' Start main program
Main:
TXState=1

' Initialize LCD DISPLAY
HIGH LCD
PAUSE 100
SEROUT LCD, LcdBaud, [LcdBLon]
PAUSE 550
SEROUT LCD, LcdBaud, [LcdCls]
PAUSE 750
SEROUT LCD, LcdBaud, [(LcdLine1), DEC 1, DEC Frequ+10700, " Mhz          "]
SEROUT LCD, LcdBaud, [(LcdLine3), "PP-002m rel. 1.0"]
SEROUT LCD, LcdBaud, [(LcdLine4), "(C) 2011 by IZ0ROO"]

' enable PLL circuit
HIGH 2

' set start frequency (144.00 Mhz)  N=166 A=40
N=166
A=40

GOSUB PLL ' calls PLL subroutine

' enable RX circuit
LOW 4  'TX OFF
HIGH 3 'RX ON
N2=180
A2=0
TXState=1

' STARTS LISTENING FOR BUTTON PRESSED

' It controls the PTT (Push To Talk) line from microphone to enable TX and disable RX
PTT:
    BUTTON pttBtn, 0, 0, 15, pttBtnWrk, 0, No_PressPTT
    IF TXState=1 THEN
       LOW 3  'RX OFF
       HIGH 4 'TX ON

       TMP=N
       N=N2

       TMP2=A
       A=A2
       GOSUB PLL

       N=TMP
       A=TMP2
       TXState=0
    ENDIF
GOTO PTT


' PTT not pressed, RX ON and TX OFF
No_PressPTT:

    IF TXState=0 THEN
      GOSUB PLL ' calls PLL subroutine

      ' enable RX circuit
      LOW 4  'TX OFF
      HIGH 3 'RX ON
      TXState=1
```

```
  ENDIF

' It controls the UP button to increase the frequency
FrequUP:
    BUTTON upBtn, 0, 100, 15, upBtnWrk, 0, FrequMID
    TXState=1

    IF Frequ=LFrequ THEN ' if low limit frequency
       A1=40             ' set register (RX) A to initial value
       A2=0              ' set register (TX) A to initial value
    ENDIF

    IF Frequ<=HFrequ-25 THEN            ' frequency < high limit
      Frequ=Frequ+25                    ' increases frequency  25 Khz


      ' RX Frequency parameters
      N1=(Frequ/800)+125  ' computes N parameter for PLL

      IF (Frequ//800)=0 THEN
         A1=0
      ELSE
         A1=A1+2
         IF A1>62 THEN
           A1=0
         ENDIF

      ENDIF

      N=N1
      A=A1
      GOSUB PLL

      ' TX Frequency parameters
      N2=((Frequ+10700)/800)+125
      IF Frequ=LFrequ THEN
         A2=0
      ENDIF

      IF ((Frequ+10700)//800)=0 THEN
         A2=0
      ELSE
         A2=A2+2
         IF A2>62 THEN
           A2=0
         ENDIF
      ENDIF

      SEROUT LCD, LcdBaud, [(LcdLine1), DEC 1, DEC Frequ+10700, " Mhz"]
    ENDIF


FrequMID:
    BUTTON midBtn, 0, 100, 15, midBtnWrk, 0, FrequDOWN
    TXSTate=1
    N2=181
    A2=16

    N1=167
    A1=56
    N=N1
    A=A1
    Frequ=34300
    GOSUB PLL
    SEROUT LCD, LcdBaud, [(LcdLine1), DEC 1, DEC Frequ+10700, " Mhz"]


' It controls the DOWN button to decrease the frequency
FrequDOWN:
    BUTTON downBtn, 0, 100, 15, downBtnWrk, 0, No_PressDOWN
    TXSTate=1

    IF Frequ=LFrequ THEN
       A1=40
       A2=0
    ENDIF

    IF Frequ>=LFrequ+25 THEN
         Frequ=Frequ-25

         ' RX Frequency parameters
         N1=(Frequ/800)+125
         IF (Frequ//800)=0 THEN
            A1=0
         ELSE
            A1=A1-2
            IF A1=65534 THEN
```

```
                A1=62
             ENDIF
          ENDIF

          N=N1
          A=A1
          GOSUB PLL

          ' TX Frequency parameters
          N2=((Frequ+10700)/800)+125
          IF ((Frequ+10700)//800)=0 THEN
             A2=0
          ELSE
             A2=A2-2
             IF A2=65534 THEN
                A2=62
             ENDIF
          ENDIF
          SEROUT LCD, LcdBaud, [(LcdLine1), DEC 1, DEC Frequ+10700, " Mhz"]
     ENDIF

     ' down button not pressed
  No_PressDOWN:
     TXState=1
     IF muting=0 THEN
          SEROUT LCD, LcdBaud, [(LcdOn1), (LcdLine2), "MUTING OFF     "]
     ELSE
          SEROUT LCD, LcdBaud, [(LcdOn1),(LcdLine2), "MUTING ON       "]
     ENDIF
     GOTO PTT


' PLL Subroutine, it sends division parameters to PLL through SPI protocol
PLL:
    SHIFTOUT DataPin, ClockPin, MSBFIRST, [1\1]     ' BIT SW
    SHIFTOUT DataPin, ClockPin, MSBFIRST, [640\14]  ' register R
    SHIFTOUT DataPin, ClockPin, MSBFIRST, [1\1]     ' bit C=1
    PULSOUT LatchEnablePin, 15

    SHIFTOUT DataPin, ClockPin, MSBFIRST, [N\11]    ' LOAD N
    SHIFTOUT DataPin, ClockPin, MSBFIRST, [A\7]     ' LOAD A
    SHIFTOUT DataPin, ClockPin, MSBFIRST, [0\1]     ' bit C=0
    PULSOUT LatchEnablePin, 15
RETURN
```

Calibration

CPU programming

Before tuning the radio, You have to upload the firmware in the CPU.

To calibrate the radio You will need the following tools:

- signal generator;
- digital frequency meter;
- VHF receiver on the working frequencies of the transceiver.

The calibration of the radio is required to obtain the best signal reception and the best signal transmission. I suggest to tune the generator at the frequency of 145 MHz, modulating the signal at 7 kHz, connect its output at the entrance of the antenna and set the signal level at 50 uV.

PLL calibration

Connect the digital frequency meter to adjust the PLL reference oscillator.

1) measure the frequency from the IC4 Pin 1;
2) adjust the C42 variable capacitor in order to obtain an 8 Mhz reading.

Receiver calibration:

Once activated, the generator, You will need to:

1) tune the generator on 145 Mhz modulating the carrier with a 1 Khz signal;
2) tune the radio on 145 Mhz
3) adjust the IFs L3 and L4 for the maximum s-meter deviation;
4) adjust the s-meter trimmer if it isn't possible to see any movement from the instrument;
5) adjust the coils L1 and L2 to increase the s-meter reading;
6) repeat the procedure from point 3 up to reach the best signal reading;
7) adjust the coil L5 to obtain the lower sound distortion.

Transmitter calibration:

1) tune the radio on 145 Mhz;
2) connect a 50 ohm load or an antenna;
3) push the PTT button;
4) adjust the C79, C75, C76 capacitors in order to obtain the maximum deviation of the s-meter;
5) adjust the VR2 Trimmer to bring the s-meter indicator up to the maximum reading;
6) adjust the VR1 modulation trimmer to get the best modulation. In this case it is necessary the use of a receiver tuned on 145 Mhz used to listen at the transmitted sound.

Components Suppliers

Parallax:	http://www.parallax.com
Digikey:	http://www.digikey.com
RF Microwaves:	http://www.rfmicrowave.it
Printed Circuit Board Manufacturer:	http://www.pcb4u.it
Coilcraft: (special thanks to "Coilcraft" for coils samples):	http://www.coilcraft.com

Software

Printed Circuit Board cad: Sprint Layout 5.0:	http://www.abacom-online.de
Schematic Diagram: TinyCAD ver.2.80.03:	http://tinycad.sourceforge.net
Parallax BS-2 PBasic Editor:	http://www.parallax.com

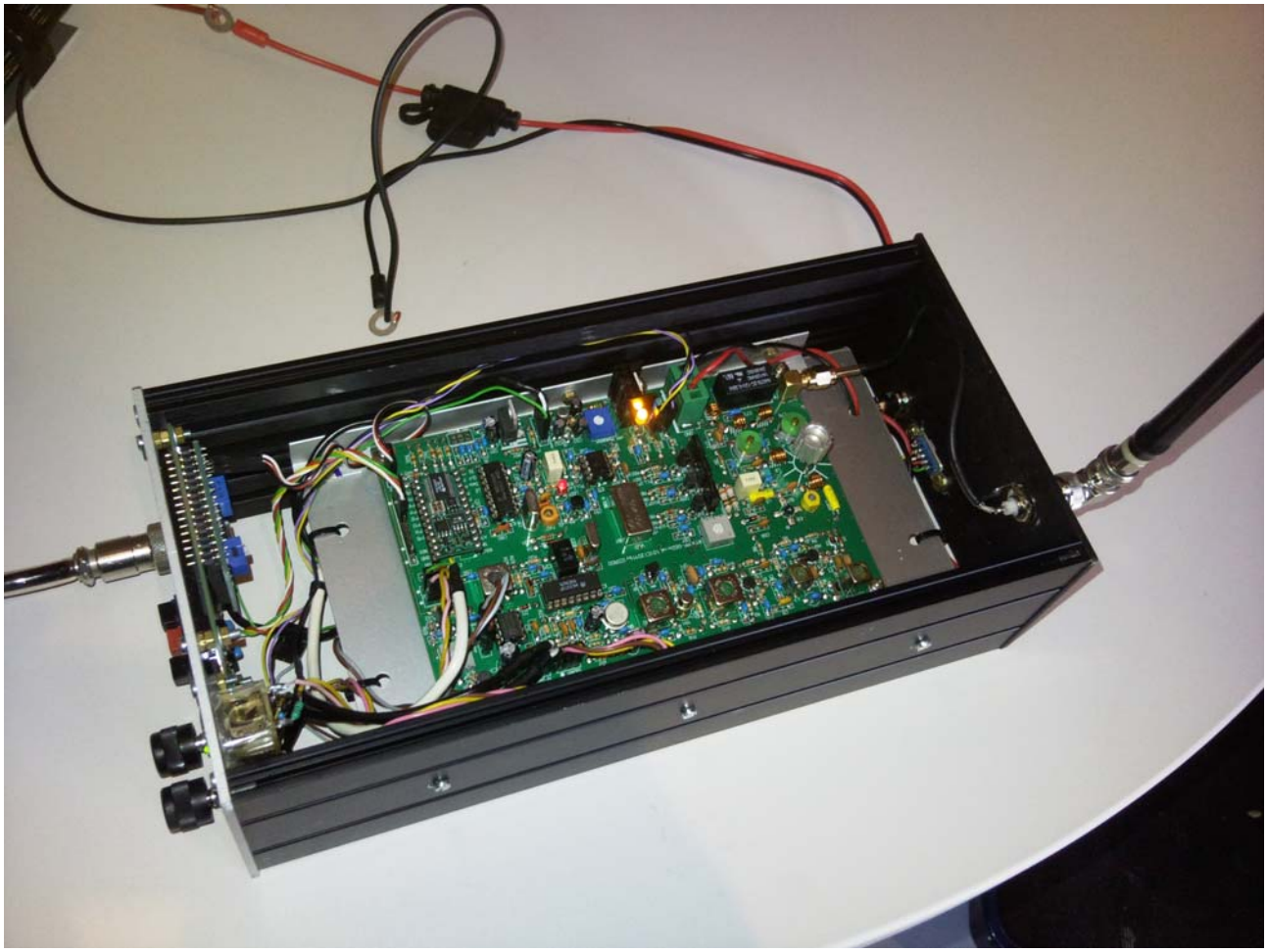
Note

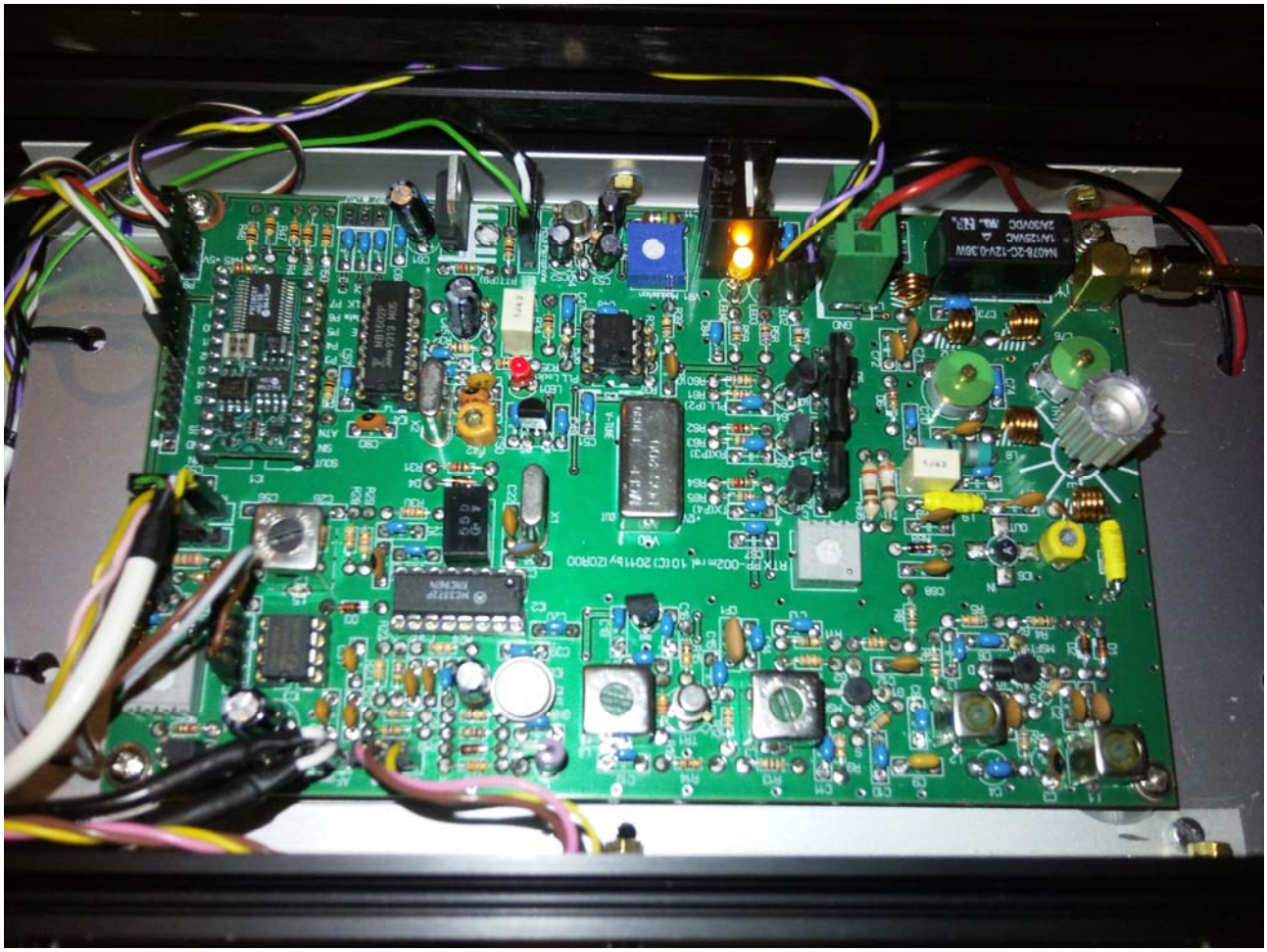
Gerber files are available on request.

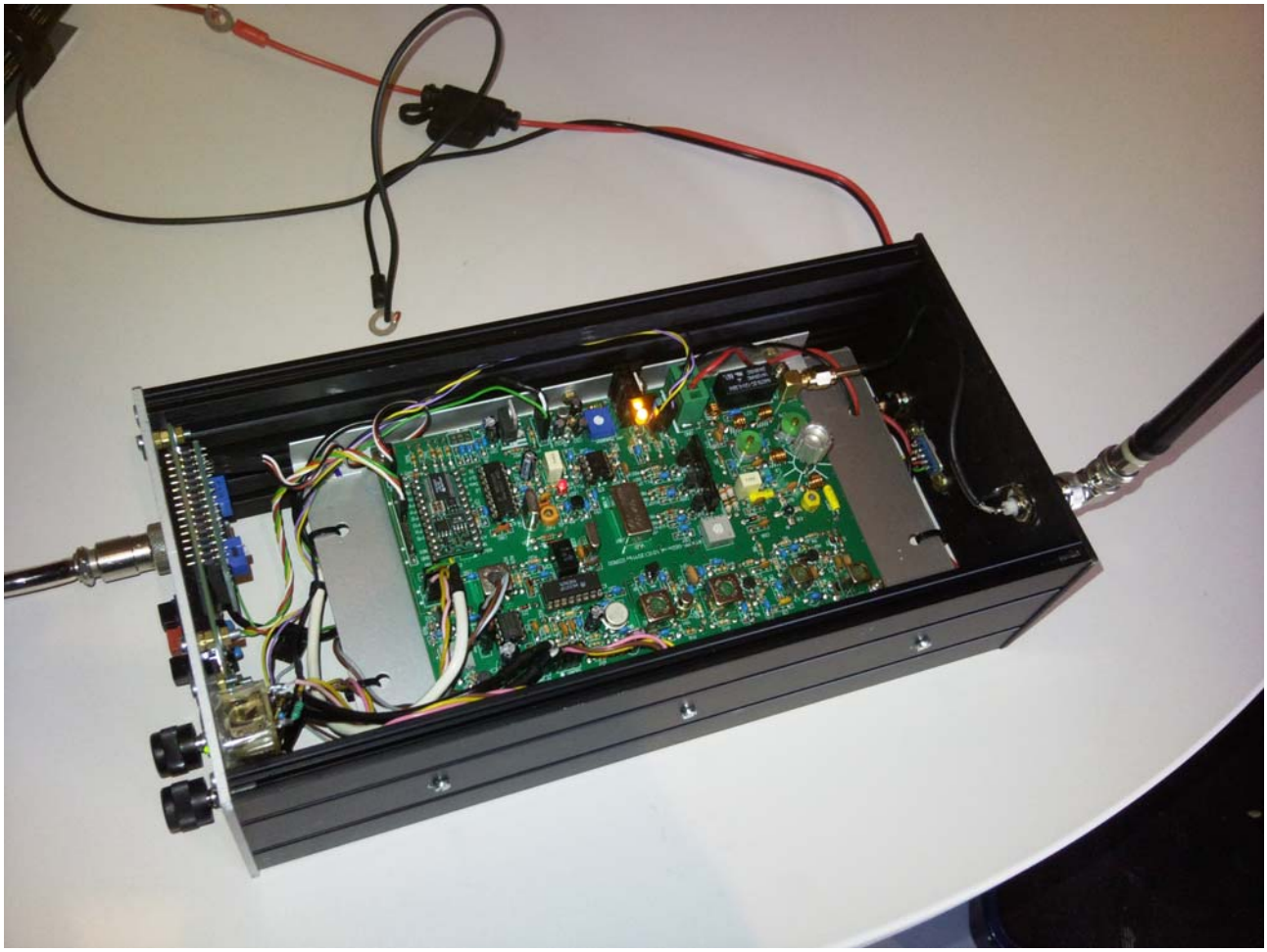
Limitation of incidental or consequential damages

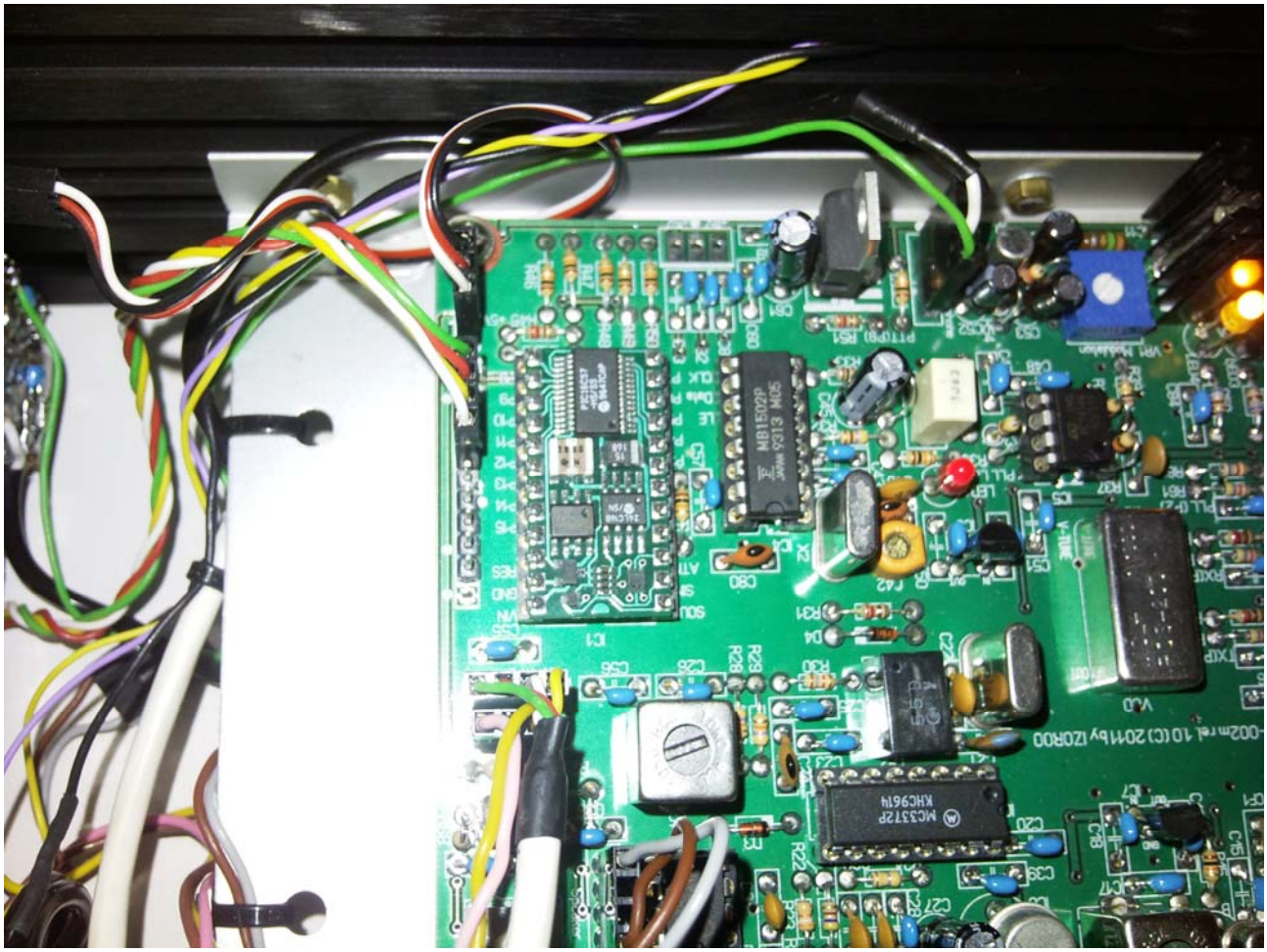
The construction of this device is the responsibility of the reader. The author will not be liable for any special, indirect, incidental or consequential damages, including but not limited to any loss of business or profits.

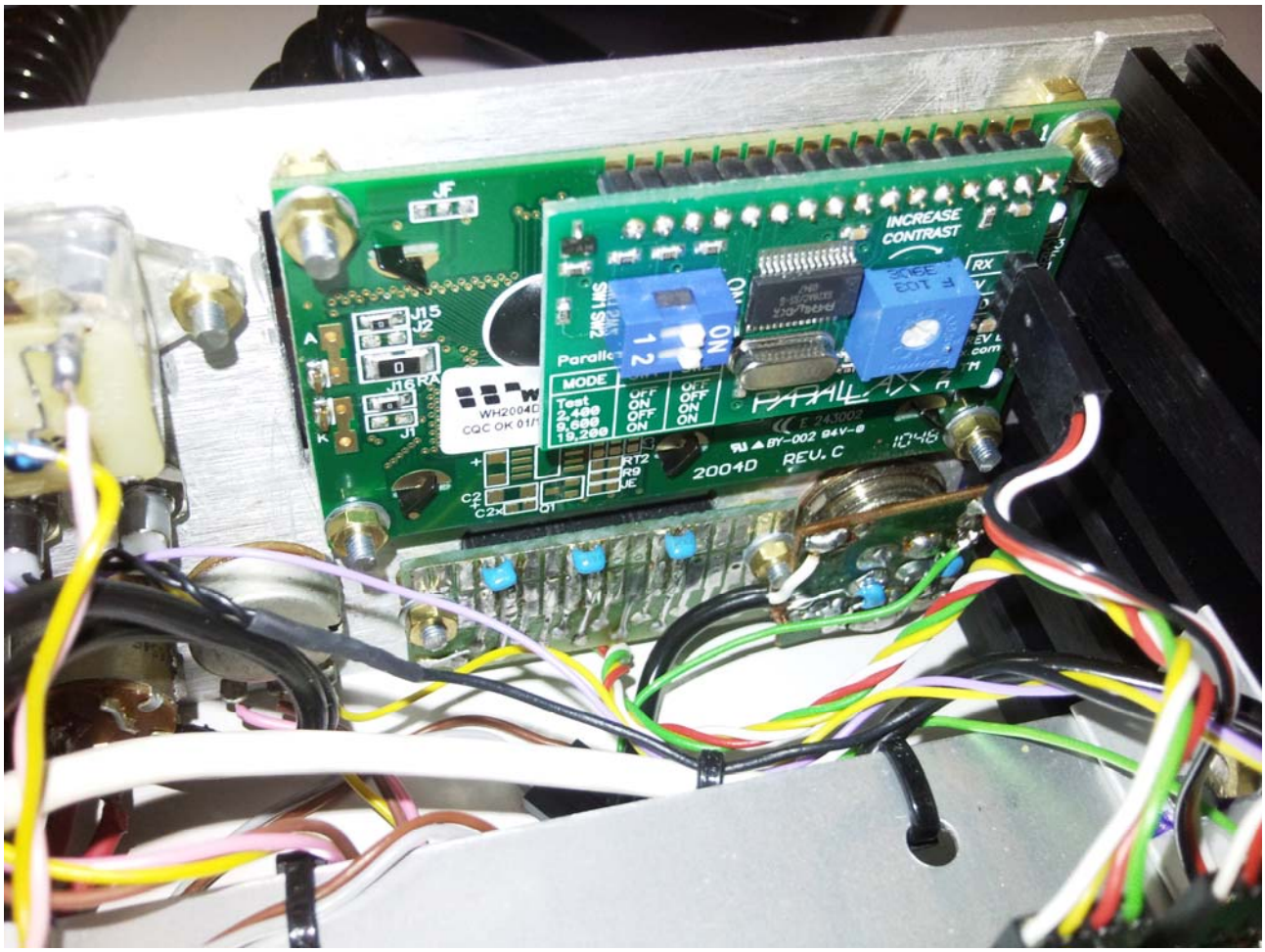
Pictures











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